REMARKS

Claims 1-20 are in the application.

The acceptance of applicant's formal drawings is acknowledged.

By this amendment, claims 1 and 17 have been amended to more particularly set out applicant's invention. FIG. 1 supports these changes. Additionally, the specification has been amended to address several minor typographical errors.

Response to 35 U.S.C. §102(b) Rejection

Claims 1, 4, 5, 7-12, 14-18, and 20 were rejected under 35 U.S.C. §102(b) as being anticipated by Blanchard USP 4,914,058 (hereafter "Blanchard"). This rejection is respectfully traversed in view the amendments made herein and the remarks presented hereinafter.

Claim 1 calls for a method of making a semiconductor vertical FET device including the steps of providing a body of semiconductor material comprising a first conductivity type, wherein the body of semiconductor material has an upper surface and a lower surface opposing the upper surface, wherein the lower surface provides a drain contact. The method also calls for forming a first trench in the body of semiconductor material and extending from the upper surface, wherein the first trench has a first width, a first depth from the upper surface, first sidewalls, and a first bottom surface. The method additionally calls for forming a second trench within the first trench, wherein the second trench has a second width, a second depth from the first surface, second sidewalls and a second bottom surface. The

method further calls for forming a first source region in the body of semiconductor material extending from the upper surface and spaced apart from the first trench. The method still further calls for introducing a dopant of a second conductivity type into at least a portion of the second sidewalls and the second bottom surface to form a doped gate region, wherein the doped gate region extends into the body of semiconductor material.

Applicant respectfully submits that the Blanchard reference fails to anticipate claim 1 for at least the following reason. Specifically, Blanchard fails to show introducing a dopant of a second conductivity type into at least a portion of the second sidewalls and the second bottom surface to form a doped gate region, wherein the doped gate region extends into the body of semiconductor material. In Blanchard, a conventional gate polysilicon layer is separated from the semiconductor substrate by a dielectric layer 32. Thus, Blanchard's gate layer is not into at least a portion of the second sidewalls and the second bottom surface as is called for in claim 1.

Claim 4 depends from claim 1 and is believed allowable for at least the same reasons as claim 1.

Claim 5 depends from claim 1 and further calls for the step of introducing the dopant of the second conductivity type comprises implanting the dopant into the second sidewalls and the second bottom surface. Claim 5 is believe allowable for the same reasons as claim 1. Additionally, applicant respectfully submits that claim 5 is allowable over Blanchard because Blanchard does not teach implanting dopant into the second sidewalls and the second bottom surface.

Claims 7-11 depend from claim 1 and are believed allowable for at least the same reasons as claim 1.

Claim 12 calls for a process for making a compound semiconductor vertical FET device including forming a first groove in a compound semiconductor layer of a first conductivity type, wherein the first groove has first sidewalls and a first lower surface, and wherein the first groove extends from a first surface of the compound semiconductor layer. The process also calls for forming a second groove within the first groove, wherein the second groove has second sidewalls and a second lower surface. Additionally, the process calls doping the second lower surface and at least a portion of the second sidewalls with a second conductivity type dopant to form a gate region. In addition, the process calls for forming a first source region of the first conductivity type in the compound semiconductor layer adjacent to the first groove. Further, the process calls for forming a source contact to the first source region, and forming a gate contact coupled to the gate region. Still further, the process calls for forming a drain contact on a second surface of the compound semiconductor layer.

Applicant respectfully submits that Blanchard fails to teach claim 12 for at least the following reasons. First, Blanchard does not teach a compound semiconductor device. Second, Blanchard does not teach doping the second lower surface and at least a portion of the second sidewalls with a second conductivity type dopant to form a gate region. In Blanchard, the gate region is separated from the sidewalls of the lower trench by a dielectric layer 32.

Claims 14-17 depend from claim 12 and are believed allowable for at least the same reasons as claim 12.

Claim 18 calls for a method for forming a compound semiconductor FET device comprising the steps of providing a

body of compound semiconductor material including a support wafer of a first conductivity type and a first dopant level and an epitaxial layer formed over the support wafer, wherein the epitaxial layer is of the first conductivity type and has a second dopant level lower than the first dopant level. The method also calls for forming a plurality of spaced apart first doped regions of the first conductivity type in the epitaxial layer, and forming a plurality of first trenches in the epitaxial layer, wherein each first trench is between a pair of first doped regions. Additionally, the method calls for forming a plurality of second trenches in the epitaxial layer, wherein one second trench is within one first trench, and doping at least portions of sidewall surfaces and lower surfaces of each second trench to form a plurality of doped gate regions, wherein the plurality of doped gate regions extend into the body of compound semiconductor material. In addition, the method calls for coupling the plurality of spaced apart first doped regions with a first contact layer, and coupling the plurality of doped gate regions to a gate connecting region. Further, the method calls for forming a drain contact a lower surface of the support wafer.

Applicant respectfully submits that Blanchard fails to anticipate claim 18 because Blanchard does not teach a method using a body of compound semiconductor material. Also, Blanchard does not teach doping at least portions of sidewalls surfaces and lower surfaces of each second trench to form a plurality of doped regions, wherein the plurality gate regions extend into the body of compound semiconductor material. As stated above, Blanchard's gate region is separated form the sidewalls and the lower surface by a dielectric layer 32.

Claim 20 depends from claim 18 and further calls for the step of doping the sidewall surfaces and lower surfaces

includes ion implanting a dopant of the second conductivity type. Claim 20 is believed allowable for the same reasons as claim 18. Additionally, applicant respectfully submits that Blanchard does not teach ion implanting a dopant of the second conductivity type to doped the sidewall surfaces and the lower surfaces.

Response to First 35 U.S.C. §103 Rejections

Claims 2, 3, 6, 13, 19 were rejected under §103(a) as being unpatentable over Blanchard in view of Plumton et al., USP 6,229,197 (hereinafter "Plumton"). This rejection is respectfully traversed in view of the amendments made herein and the remarks presented hereinafter.

Claims 2, 3, and 6 depend from claim 1. Applicant respectfully submits that the combination of Blanchard and Plumton fails to make claims 2, 3, and 6 obvious because neither reference shows or suggests introducing a dopant of a second conductivity type into at least a portion of the second sidewalls and the second bottom surface to form a doped gate region, wherein the doped gate region extends into the body of semiconductor material as is called for in claim 1.

Claim 13 depends from claim 12. Applicant respectfully submits that the combination of Blanchard and Plumton fails to make claim 13 obvious because neither reference shows or suggests doping the second lower surface and at least a portion of the second sidewalls with a second conductivity type dopant to form a gate region as is called for in claim 12.

Claim 19 depends from claim 18. Applicant respectfully submits that the combination of Blanchard and Plumton fails

to make claim 19 obvious because neither reference shows or suggests doping at least portions of sidewalls surfaces and lower surfaces of each second trench to form a plurality of doped regions, wherein the plurality gate regions extend into the body of compound semiconductor material as is called for in claim 18.

In view of all of the above, it is believed that the claims are allowable, and the case is now in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

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